L Number	Hits	Search Text	DB	Time stamp
1	7303	(nonvolatile non adj volatile) with (trench hole recess via groove opening)	USPAT;	2004/10/20 07:36
	Ì		US-PGPUB;	
			ЕРО; ЈРО	
2	868	((nonvolatile non adj volatile) with (trench hole recess via groove opening))	USPAT;	2004/10/20 06:00
	· ·	and (etch\$3 with (trench hole recess via groove opening))	US-PGPUB;	
			ЕРО; ЛРО	
3	743	(((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:00
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))	ЕРО; ЈРО	
4	433	((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:01
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
		wall) with (trench hole recess via groove opening))		
5	364	(((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:02
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
		(floating control))		_
6	320	(((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:03
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
	İ	(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
		wall) with (trench hole recess via groove opening))) and (gate near3	,	
		(floating control))) and conduct\$4		
7	317	(((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT:	2004/10/20 06:03
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	٠
		wall) with (trench hole recess via groove opening))) and (gate near3	,	
	[(floating control))) and conduct\$4) and substrate		
8	314	((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:19
U	311	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	200 11 10, 20 00.12
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
		wall) with (trench hole recess via groove opening))) and (gate near3	L10,310	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)		
9	262	(((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:06
	202	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2004/10/20 00:00
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
	ł	wall) with (trench hole recess via groove opening))) and (gate near3	L1 0, 31 0	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and silicon adj (nitride oxide)		
12	13	,	USPAT;	2004/10/20 06:07
12	13	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2004/10/20 00:07
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
		wall) with (trench hole recess via groove opening))) and (gate near3	1 110,310	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and sacrificial with (silicon adj (nitride oxide))		
11	32	((((((((((((((((((((((((((((((((((((((USPAT;	2004/10/20 06:08
	32	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2004/10/20 00:00
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
		wall) with (trench hole recess via groove opening))) and (gate near3	10,50	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))	·	٠
	}	and sacrificial		
13	183	(((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:34
13	103	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2007/10/20 00:34
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
		wall) with (trench hole recess via groove opening))) and (gate near3	1210, 310	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
14		and (expos\$4 near4 substrate)	TICDAT.	2004/10/20 06:20
14	56	((((((((((((((((((((((((((((((((((((((USPAT;	2004/10/20 06:20
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and (expos\$4 near4 substrate)) and plug	1	L

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opening)) and (etch\$3 with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and sacrificial with (trench hole recess opening) (((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expo\$4 near4 (conduct\$4) and substrate) and (dielectric insulat\$5)) and (expo\$54 near4 (conduct\$4 substrate)) (((((((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening)) and (gate near3 (floating control))) and conduct\$4) and substrate) and (silocetric insulat\$5)) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct\$4 substrate)) and plug (nonvolatile non adj volatile) with (trench hole recess via groove opening)) and (gate near3 (floating control))) and (onduct\$4) and substrate) and (silocetric insulat\$5)) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct\$4 substrate)) and (etch\$3 with (trench hole recess via groove opening)) and (gate near3 (floating control))) and (etch\$3 with (trench hole recess via groove opening					
(cieh\$3 with (photoresist resist mask\$3)) and ((spacer sidewall side adj wall) with (trench hole recess wis groove opening)) and (gate near3 (douting control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and ascendicial with (trench hole via recess pening)	10	·12	((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:27
wally with (trench hole recess via groove opening)) and (glate near3 (dloating controlly)) and conduct\$4) and substrately and (dilocting cinsulas\$5) and sacrificial with (trench hole via recess opening) 2066 (((((((((notrolatide) not vincenth hole recess via groove opening))) and (etch\$3 with (photressis resis trank\$3)) and (efchas with (photressis resis trank\$4)) and (grane raidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photressis resis trank\$4)) and (efchas with				US-PGPUB;	
wally with (trench hole recess via groove opening)) and (glate near3 (dloating controlly)) and conduct\$4) and substrately and (dilocting cinsulas\$5) and sacrificial with (trench hole via recess opening) 2066 (((((((((notrolatide) not vincenth hole recess via groove opening))) and (etch\$3 with (photressis resis trank\$3)) and (efchas with (photressis resis trank\$4)) and (grane raidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photressis resis trank\$4)) and (efchas with			(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
(Ilosting control))) and conduct(\$4) and substrate) and (dielectric insultation) and sensificial with (trench hole via recess via grove opening)) and (cetch\$3 with (photoresist resist mask\$3))) and ((epacer sidewall side aid) wall) with (trench hole recess via grove opening)) and (epacer sidewall side aid) wall) with (trench hole recess via grove opening)) and (epacer sidewall side aid) and (expost) and expost) and expost) and expost ((losting control))) and conduct\$4) and substrate) and (dielectric insultat5)) and silicon and (intrice oxide)) and (expost) and silicon and (intrice oxide)) and (expost sides the sirt oxide) and expost ((losting control))) and conduct\$4) and substrate) and (dielectric insultat5)) and silicon and (intrice oxide) and expost and expost (expost) and silicon and (intrice oxide) and expost and expost (expost) and silicon and (intrice oxide) and expost and expost (expost) and silicon and (intrice oxide) and expost and expost (expost) and silicon and (intrice oxide) and expost a near 4 expost (losting control))) and conduct\$4) and substrate) and (dielectric insulta\$5) and silicon and (intrice oxide) and exposts a near 4 expost (losting control)) and expost (expost)			wall) with (trench hole recess via groove opening))) and (gate near3		i
15			(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
15 206					
copening) and (ctch53 with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask33)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (atch54 with (photresist resist mask35)) and (atch53 with (photresist resist mask35)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask35)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask35)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask35)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask35)) and (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (ctch53 with (photresist resist mask35)) and silicon and (nitride oxide) and (expect sidewall side adj wall) with (trench hole recess via groove opening)) and plug (nonvolatile non adj volatile) with (source near4 plug) 2277 (memory) with (source near4 plug) 23	15	206		USPAT.	2004/10/20 06:34
(cich53 with (photoresist resist mask\$33)) and ((spacer sidewall side adj wall) with (french hole recess via groove opening)) and (spaces) and (expo\$4 heart (conduct\$4 substrate)) and (expo\$4 heart (conduct\$4 substrate)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (cich53 with (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (photoresist resist mask\$3)) and (spacer sidewall side adj wall) with (french hole recess via groove opening)) and (photoresist resist mask\$3)) and (spacer sidewall side adj wall) wit					200 // 10/ 20 0 14/4
wall) with (trench hole recess via groove opening)) and (gate near3 (doating control))) and conduct\$4) and substrate) and (dielectric insulat\$5) and (expos\$4 near4 (conduct\$4 substrate)) and (expos\$4 near4 (conduct\$4 substrate)) and (exch\$3 with (photoresis resist mask\$7)) and (spore seewal sid groove opening)) and (exch\$3 with (photoresis resist mask\$7)) and (spore seewal sid groove opening) and (exch\$3 with (photoresis resist mask\$7)) and (spore opening)) and (exch\$3 with (photoresis resist mask\$7)) and (spore opening)) and (exch\$3 with (photoresis resist mask\$7)) and (spore opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (exch\$3 with (proch hole recess via groove opening)) and (groove proch proc					
(floating control))) and condout\$4 substrate) ((((((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and ((space sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and ((space sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and (space sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and (space sidewall side adj wall) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3)) and (space sidewall side adj wall) with (trench hole recess via groove opening)) and etch\$3 with (photoresist resist mask\$3)) and (etch\$4 substrate))) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct\$4 substrate))) and (etch\$3 with (photoresist resist mask\$3)) and (etch\$4 with source near4 plug) 21				Li 0, 31 0	
16					,
179					
	4.5	• 70		LIODATE	2004/10/20 06 24
(etch53 with (photoresist resist mask53)) and (space reidewall side adj wall) with (french bote recess via grove opening)) and (gate near3 (floating control))) and conduct54) and substrate) and (dielectric insulat5)) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct54 substrate)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct54 substrate)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and (etch53 with (photoresist resist mask53)) and (felectric insulat5)) and silicon adj (intride oxide)) and (expos\$4 near4 (conduct\$4 substrate))) and file and plug (nonvolatile non adj volatile) with (source near4 plug)	16	179		•	2004/10/20 06:34
wall) with (trench hole recess via groove opening)) and (gate near3 (floating control)) and conduct\$4 and substrate) and (dielectric insulat\$5)) and silicon adj (nitride oxide)) and (expos\$4 near4 (conduct\$4 substrate)) (((((((((((nutoutaltie non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and plug (nonvolatile non adj volatile) with (source near4 plug) (spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and ((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (substrate) (uspArī, usp-GPUB, EPO, IPO uspArī, usp-GP					
(floating control)) and conduct\$4) and substrately and (dielectric insulat\$5)) and silion adj (intride oxide)) and (expos\$4 near4 (conduct\$4 substrately) ((((((((((((((((((((((((((((((((((((EPO; JPO	
2004/10/20 06:34					
17		'			
(etch\$3 with (photoresist resist mask\$3))) and (espacer sidewall side adj wall) with (trench hole recess via groove opening)) and and appling (nonvolatile non adj volatile) with (source near4 plug) 2004/10/20 07:20 277	17	52	((((((((((((((((((((((((((((((((((((((USPAT;	2004/10/20 06:34
(etch\$3 with (photoresist resist mask\$3))) and (espacer sidewall side adj wall) with (trench hole recess via groove opening)) and and appling (nonvolatile non adj volatile) with (source near4 plug) 2004/10/20 07:20 277			opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
wall with (trench hole recess via groove opening)) and (gate near3 (floating control))) and conduct\$4 and substrate) and silicon adj (intride oxide)) and expos\$4 near4 (conduct\$4 substrate))) and plug (nonvolatile non adj volatile) with (source near4 plug)			(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and silicon adj (nitride oxide)) and (expos\$4 near4 (conduct\$4 substrate))) and plug (nonvolatile non adj volatile) with (source near4 plug)				·	
and silicon adj (nitride oxide)) and (expos\$4 near4 (conduct\$4 substrate))) and plug (nonvolatile non adj volatile) with (source near4 plug) 20					
18					
12					
19	18	12		LISPAT.	2004/10/20 07:20
19	10	'2	(nonvolutile non adj volutile) with (source near prag)	·	200 11 10/20 01 120
19					
13 ((((((nonvolatile non adj volatile) with (trench hole recess via groove opening)) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and (goure near4 plug) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and (source near4 plug) split adj gate	10	277	(momora) with (gourge moord plug)	-	2004/10/20 07:30
1	19	1 2//	(memory) with (source near4 plug)	· · · · · · · · · · · · · · · · · · ·	2004/10/20 07.30
13 ((((((nonvolatile non adj volatile) with (trench hole recess via groove opening)) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (photroresist resist mask53))) and (spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and (source near4 plug) 21 2039 split adj gate (split adj gate) with source near plug (split adj gate) (split adj gate) with (trench hole recess via groove opening) (split adj gate) (split					
Opening) and (etch\$3 with (trench hole recess via groove opening)) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and (source near4 plug) 2039			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		2004/10/20 07:22
(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening)) and (gate near3 (floating control))) and (source near4 plug) USPAT; US-PGPUB; EPO; JPO US-PAT; US-PGPUB; EPO; JPO US-P	20	13		'	2004/10/20 07:33
2004/10/20 07:33 2004/10/20 07:34 2004/10/20					
2039 (floating control))) and (source near4 plug) split adj gate USPAT; US-PGPUB; EPO; IPO USPAT USPAT; US-PGPUB; EPO; IPO USPAT USPAT; US-PGPUB; EPO; IPO USPAT USPAT 2004/10/20 08:21 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:23 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:36 USPAT 2004/1				EPO; JPO	
2039 split adj gate USPAT; US-FGPUB; EPO, JPO USPAT US-FGPUB; EPO, JPO		İ			
22 2 2 2 (split adj gate) with source near plug					
2	21	2039	split adj gate	· · · · · ·	2004/10/20 07:33
22 2 2 (split adj gate) with source near plug	Í				
161 ((nonvolatile non adj volatile) with (trench hole recess via groove opening)) uS-PGPUB; EPO; JPO uSPAT; uS-PGPUB; EPO; JPO uSPAT		ł			
23	22	2	(split adj gate) with source near plug	USPAT;	2004/10/20 07:34
23	i i			US-PGPUB;	
and split adj gate 24				ЕРО; ЈРО	
and split adj gate 24	23	161	((nonvolatile non adj volatile) with (trench hole recess via groove opening))		2004/10/20 08:00
EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT US-PGPUB; EPO; JPO USPAT US-PGPUB; EPO; JPO USPAT USPAT 2004/10/20 08:21 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:26					
24					
US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT USPAT 2004/10/20 08:21 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:30 USPAT 2004/10/20 USPAT	24	5	"6271088"		2004/10/20 08:02
EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT US-PGPUB; EPO; JPO USPAT US-PGPUB; EPO; JPO USPAT	۱ - ۲	l	32.1130		
25					
US-PGPUB; EPO; JPO USPAT; 2004/10/20 08:21 US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:22 USPAT 2004/10/20 08:26 USPAT 2004/10/20 08:30 USPAT 2004/10/20 USPAT	25	10	"6204126"	1	2004/10/20 08-21
EPO; JPO USPAT; US-PGPUB; EPO; JPO USPAT 2004/10/20 08:21 27 1 1 USPAT 2004/10/20 08:22 28 1 1 USPAT 2004/10/20 08:22 29 0 0 USPAT 2004/10/20 08:26 30 1 USPAT 2004/10/20 08:26 31 1 1 USPAT 2004/10/20 08:26 32 1 USPAT 2004/10/20 08:26 33 1 USPAT 2004/10/20 08:26 34 1 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30	23	19	0204120		
26 8 "6143606" USPAT; US-PGPUB; EPO; JPO 27 1 USPAT 2004/10/20 08:22 28 1 USPAT 2004/10/20 08:22 29 0 0 USPAT 2004/10/20 08:26 30 1 USPAT 2004/10/20 08:26 31 1 1 USPAT 2004/10/20 08:26 32 1 USPAT 2004/10/20 08:26 33 1 USPAT 2004/10/20 08:26 33 1 USPAT 2004/10/20 08:26 34 1 USPAT 2004/10/20 08:30 35 1 USPAT 2004/10/20 08:30 36 USPAT 2004/10/20 08:30 37 USPAT 2004/10/20 08:30 38 USPAT 2004/10/20 08:30 40 USPAT 2004/10/20 08:30 40 USPAT 2004/10/20 08:30 40 USPAT 2004/10/20 08:30 41 USPAT 2004/10/20 08:30					
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31 1 32 1 33 1 34 1 35 1 36 1 37 1 38 1 39 1 31 1 32 1 33 1 34 1 35 1 36 1 37 1 38 1 39 1 30 1 31 1 32 1 33 1 34 1 35 1 36 1 37 1 38 1 39 1 30 1 30 1 31 1 32 1 33 1 34 1 35 1 36 1 37 1 38 1 39 1 30 1 30 1 30 1 30 1 30 1 30 <td>1</td> <td>1</td> <td></td> <td></td> <td></td>	1	1			
32	1	1			
33		1 -			
34 1 2004/10/20 08:30 35 1 USPAT 2004/10/20 08:30 USPAT 2004/10/20 08:30		1 7		b .	1
35 USPAT 2004/10/20 08:30	1	1			
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30 1 USPA1 2004/10/20 08:30	l .	!			
	30	<u> </u>	<u> </u>	USPAI	2004/10/20 08:30

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L Number	Hits	Search Text	DB	Time stamp
1	7303	(nonvolatile non adj volatile) with (trench hole recess via groove opening)	USPAT;	2004/10/20 05:59
			US-PGPUB;	
2	868	((nonvalatile non edi valatile) with (tuench hele masses via superio enemina))	ЕРО; ЛО	2004/10/20 06:00
2	800	((nonvolatile non adj volatile) with (trench hole recess via groove opening)) and (etch\$3 with (trench hole recess via groove opening))	USPAT; US-PGPUB;	2004/10/20 06:00
•		and (etch\$5 with (trench hole recess via groove opening))	EPO; JPO	
3	743	(((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:00
	İ	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))	ЕРО; ЈРО	
4	433	((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:01
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
_		wall) with (trench hole recess via groove opening))	1 10D . m	0004/10/00 06 00
5	364	((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:02
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB; EPO; JPO	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj wall) with (trench hole recess via groove opening))) and (gate near3	EPO; JPO	
		(floating control))		
6	320	(((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:03
· ·	320	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	200 11 10/20 00:02
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
		wall) with (trench hole recess via groove opening))) and (gate near3	ŕ	
		(floating control))) and conduct\$4		
7	317	(((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:03
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
•		(floating control))) and conduct\$4) and substrate	LIGDATE	2004/10/20 06 10
8	314	((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT; US-PGPUB;	2004/10/20 06:19
	1	opening)) and (etch\$3 with (trench hole recess via groove opening))) and (etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	EPO; JPO	
		wall) with (trench hole recess via groove opening))) and (gate near3	E1 0, 31 0	
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)		
9	262	((((((((((((((((((((((((((((((((((((((USPAT;	2004/10/20 06:06
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	•
	i	(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and silicon adj (nitride oxide)		
12	13		USPAT;	2004/10/20 06:07
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
		wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and sacrificial with (silicon adj (nitride oxide))		
11	32	((((((((((((((((((((((((((((((((((((((USPAT:	2004/10/20 06:08
••	1	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and sacrificial		
	183	((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT;	2004/10/20 06:20
13	T .	opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
13	İ	(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЛРО	
13			i	
13		wall) with (trench hole recess via groove opening))) and (gate near3		
13	٠	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
	56	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expos\$4 near4 substrate)	USPAT:	2004/10/20 06:20
13	56	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expos\$4 near4 substrate) (((((((((nonvolatile non adj volatile) with (trench hole recess via groove	USPAT; US-PGPUB:	2004/10/20 06:20
	56	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expos\$4 near4 substrate) (((((((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2004/10/20 06:20
13	56	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expos\$4 near4 substrate) ((((((((((((((((((((((((((((((((((((1	2004/10/20 06:20
	56	wall) with (trench hole recess via groove opening))) and (gate near3 (floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5)) and (expos\$4 near4 substrate) (((((((((((nonvolatile non adj volatile) with (trench hole recess via groove opening))) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	2004/10/20 06:20

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10	12	((((((((((((((((((((((((((((((((((((((USPAT;	2004/10/20 06:27
		opening)) and (etch\$3 with (trench hole recess via groove opening))) and	US-PGPUB;	
•		(etch\$3 with (photoresist resist mask\$3))) and ((spacer sidewall side adj	ЕРО; ЈРО	
		wall) with (trench hole recess via groove opening))) and (gate near3		
		(floating control))) and conduct\$4) and substrate) and (dielectric insulat\$5))		
		and sacrificial with (trench hole via recess opening)		